

REMARKS

Claims 1-14, 20 and 21 were previously pending in this application.

Claims 1-14, 20 and 21 stand rejected.

Claim 21 stands rejected under 35 U.S.C. 112.

Claims 1-14, and 20-21 stand rejected under 35 U.S.C. 103(a).

Claim 21 is cancelled, without prejudice.

Claims 1-14 and 20 are amended.

New claim 22 is added.

Support for the limitations can be found in the specification at page 7, lines 29-31 and FIG. 3F.

No new matter has been added.

Claims 1-14, 20 and 22 remain in the case.

Applicant requests reconsideration and allowance of the claims in light of the above amendments and following remarks.

Drawing and Claim Objections

The Examiner states that the drawings are objected to because the language "the gate dielectric layer and a gate electrode in claim 21 must be shown or the features cancelled from the claims. Claim 21 is cancelled.

The Examiner also states that Applicant should provide a cross-hatching of materials in FIGS. 1-3. Applicant submits herewith revised FIG. 1 with a cross-hatched metal layer 8. Although Applicant has not provided a cross-hatching of dielectric layers so as not to obscure the figures, FIGS. 1-3 will be further revised and submitted upon request by the Examiner. Accordingly, the objections are overcome.

Claim Rejection – 35 USC § 112

Claim 21 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had

possession of the claimed invention. The specification is silent regarding "the substrate comprises a gate dielectric layer and a gate electrode, claim 21, lines 1-2".

Claim 21 is cancelled, without prejudice. Thus, the rejection of claim 21 under 35 U.S.C. 112 is now moot.

Claim Rejection – 35 USC § 103

Claims 1-5, 9, 12-14, and 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable U.S. Patent No. 5,723,822 Lien ("Lien") in view of U.S. Patent No. 5,773,899 Zambrano ("Zambrano").

Claims 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lien in view of Zambrano and further in view of U.S. Patent No. 6,307,264 to Fukumoto ("Fukumoto").

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lien in view of Zambrano and further in view of U.S. Patent No. 6,369,409 to Takes et al (Takes et al.).

Claims 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lien in view of Zambrano and further in view of U.S. Patent No. 6,204,454 to Gotoh et al. ("Gotoh et al.")

The rejections are respectfully traversed.

In the present invention, for example, a first metal layer (108) is formed on the polysilicon film plate (104). A second metal layer (112) is formed on the first metal layer (108). A portion of the second metal layer (112) is arranged within the recessed area of the first metal layer (108). A passivation layer (114) is formed overlying the second metal layer (112). The passivation layer (114) has an opening that exposes a region of the second metal layer (112) as a bonding pad. The polysilicon film plate (104) is disposed directly below an exposed portion of the second metal layer 112 (i.e., the bonding pad). This structure improves the resistance of the bonding pad to stress. See FIG. 3F of the instant application and the accompanying text.

Thus, when a wire bonding process is performed on a bonding pad, the polysilicon film plate 104 can absorb the thermo-mechanical stress being applied on the bonding pad. In other words, with the bonding pad *directly overlying* the polysilicon film plate (104), the stress can be absorbed and sliding of the first metal layer 108 and the first dielectric layer (102) can be prevented, during wire bonding. See page 6, lines 4-10 of the present application.

To further clarify this aspect of the present invention, claim 1 is now amended to recite, "the bonding pad *directly overlying* the polysilicon film plate."

In contrast, in Lien, an element 105 is merely a polysilicon gate to form a transistor, not for absorbing a stress induced in a bonding pad during wire bonding as in the claimed invention. Further, the bonding pad 115 of Lien, i.e., the exposed portion of the metal layer 116, does not directly overlie the polysilicon gate 105. Therefore, the polysilicon gate 105 does not improve the resistance of the bonding pad.

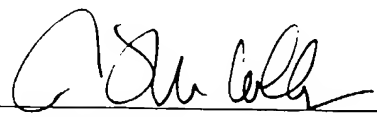
Thus, the cited references, either alone or in combination, do not teach or suggest all of the limitations of claim 1. Accordingly, the rejection does not present a *prima facie* case of obviousness. Thus, the rejection of claim 1 under 35 U.S.C 103 is improper. Therefore, claim 1 is allowable and claims 2-14, which depend therefrom and recite features that are neither taught nor disclosed in the cited references, are also allowable.

Similarly, claim 20, which recites limitations similar to claim 1, i.e., "the exposed region of the second metal layer directly overlying the polysilicon film plate," and claim 22, which depends from allowable claim 20 and recites a feature that is neither disclosed nor taught in the cited references, are allowable. In particular, none of the cited references teach or disclose, "the polysilicon film plate absorbs thermo-mechanical stress induced in the bonding pad during wire bonding," as recited in claim 22.

For the foregoing reasons, reconsideration and allowance of claims 1-14, 20 and 22 of the application as amended is solicited. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

MARGER JOHNSON & McCOLLOM, P.C.



Alan T. McCollom
Reg. No. 28,881

MARGER JOHNSON & McCOLLOM
1030 SW Morrison Street
Portland, OR 97205
(503) 222-3613

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